WHAT IS CLAIMED IS:

1. A method for forming a semiconductor package, comprising:

providing a substrate having an upper surface and a lower surface opposite the upper surface, the chip being electrically connected to the upper surface of the substrate, the substrate having a chip mounted thereon;

forming a plurality of void pads on the back surface of the chip, the voids pads being formed of a material that is non-wettable by solder;

applying a flux on the back surface of the chip, the flux including a solvent;

forming a solder preform on the flux; and

reflowing the solder preform to form voids aligned with the void pads.

2. The method of claim 1, further comprising putting a lid on the solder preform.

3. The semiconductor package of any of claim 1, wherein the voids are formed along a perimeter of the chip at uniform distances from each other.

4. The method of claim 1, wherein a copper pattern layer is formed on the back surface of the chip to expose the void pads, and wherein a nickel/gold plating layer is formed on the copper pattern layer.